2.4GHz Frequency Synthesizer

ECEN 620 Final Report

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1 Introduction

1.1 Project and Problem Statement

A 2.4GHz frequency synthesizer was designed for large spur reduction. Spurs are a serious problem in frequency synthesizers as they can degrade performance by introducing frequency components that are at the reference frequency. These components must be attenuated as much as possible so that the desired signal isn’t compromised.

1.2 Proposed Solution

Spurs appear as ripple on the control voltage line. A duplicate signal with the same frequency spectrum as the control voltage is subtracted from the control voltage to create a new VCO input signal that is devoid of frequency components other than the DC value. In theory, it can be possible to attenuate all spurs regardless of the loop bandwidth if the implementation can create an exact replica of the spurs and be able to subtract only the frequency components without affecting the DC value of the control voltage. This work investigates such a solution and analyzes the shortcomings and challenges of implementing this solution.

1.3 Phase Locked Loop (PLL) Design Specifications, Power Supply and Clock Reference

The PLL was designed to have an output frequency of 2.4GHz with a 6MHz frequency step. The VCO was also designed to have a tuning range of 5% creating a need for a frequency divider whose N ranges from 400 to 420. This frequency divider was designed as a macro-model while transistor level blocks for the charge pump, phase detector, and voltage controlled oscillator (VCO) were implemented. A reference clock signal of 6 MHz was implemented using an ideal voltage source for simulation and a power supply of 0.9 to -0.9V was used. The PLL was designed using 200nm technology.

1.4 Scope

The document is organized as follows. After the introduction, a description about the PLL sub-blocks is discussed. Then, the spur reduction technique is presented and the simulation results are shown. Finally, a conclusion section is given to discuss the results, shortcomings of the proposed solution and future challenges.
2 Frequency Synthesizer Design

2.1 Phase Detector

The schematic of the phase frequency detector used is shown in Figure 1.

![PFD Schematic](image)

This phase frequency detector uses dynamic logic that can operate at very fast frequencies with a detection range of 360 degrees. For a common phase frequency detector, problems like dead zone and blind zone will occur as the two input waveforms rise or fall at very close times. The dead zone is caused because the reset signal does not have enough time to respond to this fast transition. The blind zone is caused when the phase offset is about 360 degrees so that the leading signal is mistakenly interpreted as the lagging. The timing waveform in Figure 2 illustrates this problem. This effect causes a reduction in the phase offset detection range.

![Blindzone Effects](image)
To avoid the deadzone problem, two delay cells are inserted before the VCO and Vref inputs to allow time for reset response. With such an improvement, the detection range can be remained at 360 degree even to the frequency of more than 1.5GHz. The waveform of the PFD with and without the delay improvement is shown in Figure 3.

![Figure 3: PFD Phase Detection Range](image)

The detection range can be extended to almost 360 degree with a flattened UP-DN signal extension beyond 330 degree. This is still better than a loss of detection at large phase offset, since what we care most is the polarity for the VCO frequency to make adjustments rather than then linearity of the response.

The output example of the phase detector functionality is shown in Figure 4:

![Figure 4: PFD Timing Waveform](image)

### 2.2 Charge Pump

#### 2.2.1 Charge Pump Used in the Frequency Synthesizer

The charge pump implemented is the single-ended one discussed in class. The schematic is shown in Figure 5. The charge pump uses 30µA current sources and uses an ideal op amp for glitch suppression.
For the single-ended charge pump, even if the current mismatch is reduced to its extreme values, the current variations due to glitches may still drive the output voltage to contain spurs. An example of charging and discharging currents with this structure exhibiting glitches is shown in Figure 6.

It's apparent that minimizing these glitches will suppress the spurs even further. In the next section a newly designed charge pump is presented that will minimize these issues further however due to time, this charge pump wasn’t implemented into the loop.

### 2.2.2 New Charge Pump Idea for Suppressing Spurs. Not Implemented in Frequency Synthesizer

The differential charge pump presented in [3] reduces the high and low speed glitches encountered with the single ended charge pump described above. In this work, when the output voltage goes too low, another current branch is used to inject current into the biasing node to increase the biasing voltage so as to compensate the current
decrease. However, two problems still remain unsolved. The first problem is the output current peaking at low output voltages because the injected current is a nonlinear function of the output voltage. The second problem is the output current still goes down after the peaking since the drain source voltage of the NMOS current source goes too low while the gate voltage only increases a little bit. The condition is better demonstrated with Figure 7 simulated results for the single-ended version of the charge pump to show the charging and discharging current vs the output voltage. An ideal CMFB circuit was used for this simulation.

To solve this problem, another feedback loop is used to set the NMOS current source output to be as constant as possible. The rail to rail op amp can modify the current source gate voltage from VSS to VDD to extend the output voltage range to its maximum. The proposed circuit is shown in Figure 8.

![Figure 7: Charging and Discharging Current Vs the Output Voltage (Single-Ended)](image)

![Figure 8: Charge Pump Reducing Current Peaking Schematic (Single-Ended)](image)

The result for charging and discharging current is shown in Figure 9.
To make a better comparison this output current is also simulated in the differential charge pump with the ideal common mode feedback circuit. The results is shown in Figure 9: Charging and Discharging Current Improvement.

It’s observed that the peaking has been reduced in both cases by providing a more constant output current. However, future testing will need to implement the CMFB circuit transistor level to achieve accurate results. If this current peaking can be implemented, the spurs can be reduced even further.

2.2.3 Charge Pump Rail to Rail Op Amp

The Op Amp used in the output current reduction circuits (both single and differential) is rail-to-rail whose schematic are shown in Figure 11. To match the output current for a desired output voltage range, the Op Amp must maintain a constant large gain over a wide range of input voltage. The compensation resistor is used to move the zero to
cancel the output pole. The frequency response simulation results are shown in Figure 12. A gain of around 90dB with a phase margin of 48 degree was achieved. The GBW for the Op Amp is around 170MHz which is enough for the application in charge pump.

Figure 11: Rail to Rail Op Amp

Figure 12: Op Amp Frequency Response
2.3 Loop Filter

A third order loop filter is implemented to suppress the spurs more than the second order. Using the same unity gain frequency and open loop phase margin, Figure 15 shows that more attenuation is given at higher frequencies. Refer to a third order filter is given in Figure 13.

![Third Order Filter Schematic](image)

Due to the extra low pass filter, another pole is added to the system to give extra attenuation for the spurs as it leads to a sharper rolloff in the gain curve of the bode plot. The equations used for determining the time constants and hence the values for the resistors and the capacitors are based on the paper [4]. The basic transfer function for a third order filter is given as:

\[ F(s) = \frac{(1 + s \cdot t4)}{s \cdot t3 \cdot (1 + s \cdot t5) \cdot (1 + s \cdot t6)} \]

Using the desired phase margin, attenuation, and unity gain frequency, the poles and zero frequencies can be determined and then the component values. The relationship between desired attenuation and the component values is provided in the following equations as reported in [4]:

\[ n = \frac{\omega_s \cdot \cos(PM) - \sqrt{2 - 2 \sin(PM)}}{\sin(PM) - 1} \]

n is a value which represents the maximum degree of attenuation a PLL design can attain. The \( \omega_s \) is the frequency step offset and \( \omega_n \) is the loop unity gain frequency, and PM is the desired phase margin. For the attenuation in terms of dB is given in:

\[ \text{Atten} = 20 \log(1 + n^2) \]

For choosing an n that is less than the max, the component values can be determined by first solving for the various time constants given from the filter transfer function above:

\[ t6 = \frac{n}{\omega_s} \]
\[ t5 = \frac{\omega_s \cdot \cos(PM) - \omega_n \cdot n \cdot (1 + \sin(PM))}{\omega_n \cdot [\omega_s \cdot (1 + \sin(PM)) + n \cdot \omega_n \cos(PM)]} \]
\[ t3 = t0 \sqrt{\frac{(1 + \omega_n^2 t2^2)}{(1 + \omega_n^2 t5^2)(1 + \omega_n^2 t6^2)}} \]
\[ t0 = \frac{K_gK_v}{N \cdot \omega_n^2} \cdot (\tan(PM) + \sec(PM)) \]
Knowing the time constants the resistor and cap values can be solved. In order to achieve positive values for the each element, \( C_1 \) is set according to:

\[
\frac{t_3 \times t_6}{t_4} < C_1 < \frac{t_3 \times t_5}{t_4}
\]

Then the other elements can be solved using:

\[
t_4 = R_2 \times C_2
\]
\[
t_3 \times t_5 \times t_6 = C_1 \times C_2 \times C_3 \times R_2 \times R_3
\]
\[
t_3 \times (t_5 + t_6) = R_2 \times C_2 \times (C_1 + C_2) + R_3 \times C_3 \times (C_1 + C_2)
\]
\[
t_3 = C_1 + C_2 + C_3
\]

Using these equations, the values for the loop filter were found. Solving for these equations to achieve a bandwidth of 30kHz yields the following values in Table 1.

<table>
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<td>C1</td>
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<td>C2</td>
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<tr>
<td>R2</td>
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<tr>
<td>R3</td>
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The corresponding step response and open loop response was simulated using Matlab and given in respectively. The estimated settling time is 40\(\mu\)s and the phase margin is 45\(^\circ\). Refer to Appendix 6.1 for the Matlab code.

Figure 14: Error Loop Step Response
Figure 15: Open Loop Transfer Function
2.4 Voltage Controlled Oscillator

For the VCO design, an LC VCO was chosen to meet the phase noise requirement. The schematic of the VCO is shown in Figure 16. It is an LC cross-coupled differential VCO with both PMOS and NMOS latches, which generate negative resistance to cancel losses in the LC resonator. Since the turning range is demanded to be 5%, the frequency range that the system can handle is over 120MHz. For our application, the frequency range goes from 2.4GHz to 2.52GHz. From the perspective of reducing noise and spur, the VCO gain should be reduced. However, for a fixed frequency range, if the VCO gain is very small, it may be too hard for the charge pump to handle the large control voltage range as this design. Generally considering these issues, an accumulation-mode PMOS varactor is used for better linearity. The resonator consists of two 4nH inductors, two fixed capacitors and accumulation-type PMOS varactors. A VCO gain to be around 200MHz/V and the control voltage range for the desired frequency range is from -272.83mV to 365.87mV.

![Figure 16: VCO Schematic](image)

![Figure 17: VCO Output Frequency vs Vcontrol](image)
Phase noise of VCO and the output buffer is simulated using PSS and Pnoise, and the result is shown in Figure 18 with a result of -121.5dBc at 1MHz offset.

The time for the VCO to start simulation in the loop is also measured in transient simulation which is around 16ns as displayed in Figure 19.
2.5 Frequency Divider and Frequency Step Results

For frequency divider, a macro model coded with Verilog-A was used. It functions well to tune the N from 400 to 420 corresponding to a frequency change from 2.4G Hz to 2.52G Hz. The step simulation from 2.4G Hz to 2.448G Hz and VCO control voltage are shown in Figure 21 and Figure 20 respectively.

Figure 20: Vcontrol for Frequency Step

Figure 21: Frequency Step from 2.4GHz to 2.448GHz

2.6 Frequency Synthesizer Locking at 2.4GHz

Transient

All the building blocks designed above were placed in close loop and a transient simulation was run. Results show that the settling time is around 40us and at a value around 343mV which is expected for the 2.4G VCO output. DFT results are shown in Fig 22 and we can see that we achieve a spur of around -80dBc at 6MHz offset and -90dBc at 12MHz offset.
3 Spur Reduction Solution

3.1 Origin of Spurs

Spurs are the result of current mismatch in the charge pump and glitches on the voltage control line. These issues are periodic in nature and occur at the same frequency as the reference signal. In typical communication systems, a bandpass filter is used to attenuate all the unwanted frequency components except that of the desired signal. However, bandpass filters are not ideal and a certain bandwidth where frequencies around the fundamental are passed. This is why it is important to minimize spurs so that the signal isn't degraded. Solutions to spur reduction have included techniques to minimize the charge pump current mismatch as shown in our charge pump, lowering bandwidth with a third or even higher order filter, and also implementing system level topologies that suppress spurs by creating a higher frequency spurs in the control voltage line that aren’t located at the reference frequency. The design proposed attempts to eliminate spurs through a cancelling technique explained below.

3.2 System Level Spur Cancellation Explanation

The spur on the control voltage by cancelling it with the spur generated from a second charge pump. However, phase error information must be retained. Therefore, the solution needs a way to generate a spur wave which is centered at 0VDC as to not kill the filter DC value when the cancelling occurs.
Two charge pumps in the PLL are used. Only one of them is working during frequency and phase acquisition while the other is disabled with output voltage shorted to ground. The second charge pump begins to work after the system is locked. Whether the system is locked or not can be detected by a digital lock detector. Since the second charge pump begins to work after the system is locked, it does not have phase error information at all and contains only a spur wave around 0VDC. Since the charge pump has the same structure, their input UP and DOWN signal and the filters are exactly the same. However they have different DC components, one at the voltage for a desired VCO output frequency, the other at 0 dc voltage. So these two signals are subtracted and the control voltage contains fewer ripples without harming the phase error information.

To test our idea in transistor level, the proposed circuit in Figure 23 is added. Since the VCO is not the key issue in terms of spurs (VCO gain fixed), an ideal VCO from adhllib (with amplitude of 0.9V and VCO gain of 200MHz/V) to help us test the idea more efficiently. A second order filter was implemented in order to cut simulation test time.

![Figure 23: Spur Suppression Method Test Circuit](image)

### 3.3 Simulation Results

![Figure 24: Spur Cancellation Circuit Not Included](image)

![Figure 25: Spur Cancellation Circuit Included](image)
Figure 24 and Figure 25 above show the Fourier Transform of the output signal. The spurs are located at intervals of 6MHz. There is essentially a great reduction of spurs at the output. Also, by observing the VCO input signal after 45µs, the additional circuit turns on, and the spurs and glitches are canceled quite well. The method proposed helps to reduce spur of more than 6dB.

![Figure 26: VCO Input. Transition of Cancelling Circuit Turning ON](image)

### 4 Conclusions

#### 4.1 Design Summary

A 2.4G frequency synthesizer for wireless communication is designed using 0.2um technology with frequency tuning range from 2.4GHz to 2.52GHz. Key building blocks, Phase and Frequency Detector, Charge pump and Voltage controlled oscillator are all implemented in transistor level. A third order filter is adopted and carefully designed using Matlab. Phase noise of -121.5dBc@1MHz (VCO part only) and spurs of around -81dBc@6MHz are achieved. Two spur suppression techniques are implemented in Macro-model. Simulation results in Cadence show that the spur performance improved 6dB.

#### 4.2 Limitations Encountered

The main design challenge for this project is the high spur requirement. The requirement is even higher than some published results in JSSC and ISSCC. Though we used an ideal frequency divider and try some spur suppression technique, we still cannot meet this requirement in transistor level PLL.

The other challenge is that the simulation time for the PLL takes too long. Though using macro-model and changing toleration or algorithm of simulator can help us to
get the result faster, it seems that the more conservative we simulate the better results we get. So there is a tradeoff between the time of waiting simulation and the quality of the simulation result.

The drawbacks of this method is also obvious. The phase noise performance degrades as the additional charge pump and filter contribute more noise. This issue may be even more serious when practical switches are used instead of the ideal ones.

Another problem with the circuit is the condition at which the control voltage settles at a non-zero value. This means that after the system settles, the dc voltage on the main filter and the spur cancelling filter is different. Thus, the current mismatch condition of the two charge pumps are not the same. Though the system will not be out of lock, it will have more low-frequency noise on the control voltage, thus more in-band noise. This is a key issue to be solved in further research. This problem is exemplified from using a transistor level VCO whose corresponding control voltage for 2.4GHz is no longer 0VDC but 343mV. The result is not good as shown in Figure 27. Though the spur may be reduced a little bit, the benefits are canceled by the bad noise spur.

![Figure 27: Control Voltage with Transistor Level VCO](image)

4.3 Future Work

We need to further our research on the two spur suppression techniques presented. First for the reduction of the output current peaking in the charge pump and second for the spur cancellation technique. For the first spur subtraction technique, we need to come up with some solutions to deal with the different current mismatch condition of the two charge pump when the control voltage settles at a non-zero value. For the second spur averaging technique, we need to figure out a way to simulate the proposed circuit. Since for now, both of the two techniques are described in macro-model, we should devote to implement them in fully transistor level and solve the problems that come with that. Specifically, implementation of the Charge Pump
Common Mode feedback and a circuit that can be used to accurately add the negative spurs with the positive ones while not introducing more problems in locking or phase information.
5 References


6 Appendix

6.1 Matlab Code for Filter Values

```matlab
% 4th Order PLL
%
% Compute Time Constants
% zero is t1, Kf=t0, pole is t2
PM = 0.5*pi/2;
wn = 30e3*2*pi;
Kv = 200e6;
Kd = 30e-6/(2*pi);
%Kd = 5e-3;
N=400;
% max attenuation factor
ws=6e6*2*pi;
nmax=ws/wn*(cos(PM)-sqrt(2-2*sin(PM)))/(sin(PM)-1);
n=0.2;
atten = 20*log10(1+(n)^2);
t5=(ws*cos(PM)-n*wn*(1+sin(PM)))/(wn*(ws*(1+sin(PM))+n*wn*cos(PM));
t4=(tan(PM)+sec(PM))/wn;
t6=n/ws;
t0=Kd*Kv/(N*wn^2)*(tan(PM)+sec(PM));
t1=(tan(PM)+sec(PM))/wn;
t2=1/(wn*tan(PM)+wn*sec(PM));
t3=t0*sqrt((1+wn^2*t2^2)/((1+wn^2*t5^2)*(1+wn^2*t6^2));
% Create Filter
s = tf('s');
F=1/(s*t3)*(1+s*t4)/(1+s*t5)*(1+s*t6);
C1=25e-12;
R3=-t3*t5*t6*(C1*t4^2-t3*t5*t6)/(t4*C1*((t4+C1-t3*t5)*(t4*C1-t3*t6));
R2=t4*(C1*t4^2-t3*t5*t6)/(t3*C1*((t4^2+t5*t6)-t4*(t5+t6));
C3=-(t4*C1-t5*t3)*(C1*t4-t3*t5)/(C1*t4^2-t3*t5*t6);
C2=t3*C1*(-t4+t5)*(-t4+t6)/(C1*t4^2-t3*t5*t6);
Aloop = (Kv*Kd*F)/(N*s);
T = N*Aloop/(1+Aloop);
figure(1)
bode(Aloop);
hold on;
figure(2);
E = 1/(1+Aloop);
step(E);
```