3 ppm Ultra Wide Range Curvature Compensated Bandgap Reference

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Abstract—In this report a current mode bandgap with a temperature coefficient of 3 ppm for the range from -117°C to 144°C is presented. 2nd order curvature compensation is used by using a third BJT with a temperature constant current and a second error amplifier to get a nonlinear temperature coefficient current in extra to enhance the accuracy. The required minimum supply voltage is 1.3V for 3ppm and 1.2V for 10ppm TC. The circuit has a line regulation of 0.86mV/V, PSRR of -57dB at 100Hz and -56dB at 1kHz. The bandgap core dissipates 22uA current and the error amplifier dissipates 3uA each. The process used is tsmc 0.18µm. The chip area is estimated as 280µm × 260µm. Process variation and mismatch as well as amplifier offset voltage effects are simulated. A resistor trimming circuit of 4 bits is made to compensate for the variation and mismatch to as much as ±5%.

I. INTRODUCTION

Temperature independent reference voltage are in need in many circuit applications such as LDO reference voltage, ADC reference voltage, and memories. To achieve a temperature independent voltage, usually a proportional-to-absolute-temperature (PTAT) voltage and a complementary-to-absolute-temperature (CTAT) voltage are summed with weighting factors to cancel their temperature coefficient (TC) so that to get a first order temperature independent voltage reference. As the Vbe voltage has less variation than the threshold voltage and mobility of MOSFETs BJT based voltage references are more popular than those based on MOSFET Vgs voltages. However standard CMOS only have access to the lateral pnp BJT with the collector fixed to the P-substrate as a trade-off. Bipolar Junction Transistors (BJT) are used to generate the PTAT voltage by using the Vbe as PTAT voltage and ΔVbe as CTAT voltage. An error amplifier is often used to force two voltages equal as in the following figure. If a more flexible output voltage is required, then current mode bandgap reference can be used which consists of a PTAT current and a CTAT current. Two MOSFET operating in subthreshold can provide similar characteristics by using two Vgs but with more variation. The weighted sum of PTAT and CTAT current is a temperature independent current which goes through a resistor to be converted back to voltage. However, the limit for the first order cancellation is typically around 20ppm to 100ppm. (author?) [5] To achieve better temperature coefficient, higher order cancellation techniques are needed.

II. BACKGROUND AND PREVIOUS WORK

For the traditional voltage mode bandgap in Figure 1,

\[ V_{REF} = \Delta V_{BE} + V_{BE} \]

The MOSFETs have the same sizing so that they are forced to have the same current. The polarity of the error amplifier is chosen so that the right hand negative feedback loop has a larger gain than the right hand positive feedback loop.

\[ LG^- = A_{amp} \cdot g_{m,PMOS} \cdot (R_{O,PMOS}|(R_1 + g_{m,Q2}) \]

\[ LG^+ = A_{amp} \cdot g_{m,PMOS} \cdot (R_{O,PMOS}|(R_2 + g_{m,Q1}) \cdot \frac{g_{m,Q1}}{R_2 + g_{m,Q1}} \]

Since \( g_{m,Q1,0} \gg R_{O,PMOS}, R_1, R_2 \), it’s easy to know \( LG_{DC,Negative} > LG_{DC,Positive} \).
For the traditional current mode bandgap in Figure 2,
\[ I_{REF} = \frac{\Delta V_{BE}}{R_1} + \frac{V_{BE}}{R_2} \]

The MOSFETs have the same sizing so that they are forced to have the same current. The polarity of the error amplifier is chosen so that the left hand negative feedback loop has a larger gain than the right hand positive feedback loop.

\[ LG^- = A_{amp} \cdot g_{m,PMOS} \cdot (R_{O,PMOS}||R_3)||R_1 + g_{m,Q2}) \]
\[ LG^+ = A_{amp} \cdot g_{m,PMOS} \cdot (R_{O,PMOS}||R_2)||g_{m,Q1}) \]

Since \( g_{m,Q1}g_{m,Q2} < R_{O,PMOS} \), \( R_1, R_2 \), it's easy to know \( LG_{DC, Negative} > LG_{DC, Positive} \).

Many higher-order cancellation techniques are developed to achieve better cancellation, such as quadratic temperature cancellation, exponential temperature cancellation, piecewise linear curvature correction. Among these techniques, a 2nd order curvature cancellation by a third BJT with a first order linear curvature correction. Among these techniques, a 2nd order cancellation, exponential temperature cancellation, piecewise to achieve better cancellation, such as quadratic temperature coefficient can be as low as around 2ppm. In (author?) [2] even a fourth BJT is used to further extend the compensation range. However, no significant improvement of accuracy can be seen from this work as the TC is 3.9 ppm in the best case. The bandgap uses cascode structure to improve PSRR but it also limits the minimum supply voltage. In (author?) [1] MOSFET ratio is used to cancel the two BJT temperature coefficient. The output node implements a super source follower which can even drive resistive load. However, only first order cancellation accuracy can be achieved using this structure and MOSFET mismatch is also more difficult to control than resistor mismatch which can be trimmed easily using binary weighted resistor string with MOSFET switches.

### III. PROPOSED CIRCUIT STRUCTURE

![Diagram of the proposed bandgap reference circuit](image-url)

Figure 3. Proposed Bandgap Reference

The proposed bandgap reference uses only three BJTs to save power while also making the design complexity lower. Self-Cascode structure is used in the bandgap core circuit to save supply voltage headroom. The error amplifier also uses self-cascode structure to enhance DC gain while keeping supply voltage low.

### IV. DESIGN PROCEDURE AND COMPONENT SIZING

1) To determine proper current of the left two BJTs, ideal VCCS and ideal OpAmp (VCVS) are used to get the temperature coefficients of the Vbe, \( \Delta V_{BE} \) and \( I_{PTAT} \) through the BJTs.
2) $I_{CTAT}$ is obtained by the formula $I_{CTAT} = \frac{V_{be}}{R_2}$. R1 and R2 are chosen so as to compensate the TC to the first order.

3) $I_{PTAT}$ and $I_{CTAT}$ are summed to get $I_{Const}$ flowing through Q3. $V_{NL}$ is obtained as $V_{NL} = V_{be,Q1} - V_{be,Q3}$ and $I_{NL}$ is then defined as $I_{NL} = \frac{V_{NL}}{R_3}$.

4) TCs of $I_{CTAT}$ and $I_{NL}$ are compared and R3 is chosen to compensate the TCs of the two currents to the second order.

5) Do optimization in cadence on R2 and R3 to get the minimum voltage variation.

6) Set $R_{OUT}$ to a proper value so that $V_{OUT}$ equal the average value of $V_{be,Q1}$ to get a minimum $V_{DS}$ variation.

7) PMOS sizes are chosen based on $I_{CTAT}$, $I_{PTAT}$ and $I_{Const}$.

8) Design the error amplifier to have sufficient gain for good PSRR.

As tsmc 0.18µm technology exhibits short channel effects, square law calculation cannot be used in actual BJT and MOSFET sizing. Iterations have to be done to optimize the circuit performance. But the above analysis can still serve as a guideline to fix the sizes of transistors.

Table I shows the value of the resistors and sizes of the MOSFET transistors of the bandgap core circuit.

Table II shows the value of the resistors and sizes of the MOSFET transistors of the error amplifier.

Table III gives a comparison of this bandgap reference with some other published works. It can be seen that the wide temperature range makes the circuit suitable for even extreme cases like space exploration, continental shelf exploration or some weaponry application.

As shown in Figure 6, the minimum supply voltage required for this bandgap is only 1.3V and the output voltage is 820mV. A line regulation of 0.86mV/V is achieved.

The output noise of the BGR is shown in Figure 7. The total integrated output noise is 0.9mV.

The power supply rejection of the bandgap reference is shown in Figure 9. The PSR at 100Hz is -57dB and at 1kHz is -56dB. The main contributor of the PSR is the error amplifier gain. The frequency response of the error amplifier is also shown in Figure 10 for a comparison.

Table III gives a comparison of this bandgap reference with some other published works. It can be seen that the
Table III

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<tbody>
<tr>
<td>Technology</td>
<td>0.18µm CMOS</td>
<td>0.18µm CMOS</td>
<td>0.6µm CMOS</td>
<td>0.35µm CMOS</td>
<td>0.35µm CMOS</td>
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<tr>
<td>Supply Voltage</td>
<td>1.3V~4V</td>
<td>1.1V~1.8V</td>
<td>0.98V~1.5V</td>
<td>0.9V~4V</td>
<td>1.5V~4.3V</td>
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<tr>
<td>Current Dissipation</td>
<td>28µA</td>
<td>&lt;14µA</td>
<td>&lt;18µA</td>
<td>0.055µA</td>
<td>0.11µA</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>820mV</td>
<td>1.012V</td>
<td>603mV</td>
<td>891mV</td>
<td>670mV</td>
</tr>
<tr>
<td>TC (ppm/°C)</td>
<td>3</td>
<td>4</td>
<td>15</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>PSRR @ 100Hz</td>
<td>-56dB</td>
<td>-75dB</td>
<td>-44dB</td>
<td>-59dB</td>
<td>-47dB</td>
</tr>
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VI. PROCESS VARIATION AND RESISTOR TRIMMING

Although the resistors in the circuit exhibit process variation which can make the actual circuit inaccurate when fabricated, resistor trimming can still be done after fabrication to compensate for resistor variation and mismatches. Assuming a process variation of 10%, Figure 11 shows that global process variation makes the worst case TC of 9 ppm, which is often

![Figure 7. Bandgap Output Noise](image7.png)

![Figure 8. Bandgap Chip Area Estimation](image8.png)

![Figure 9. Power Supply Rejection](image9.png)

![Figure 10. Error Amplifier Frequency Response](image10.png)

performance of this bandgap reference is comparable with these published works.
within the tolerance. However a mismatch between different resistors of 5% can make the TC as bad as 64 ppm as shown in Figure 12, which can be untolerable. As a result, a trimming circuit with 4 bits input to cover a range of 5% compensation is used to make the target resistor approach its nominal value to within 0.3% as in Figure 13. The trimming is only used for two resistors \( R_1 \) and \( R_2 \) for mismatch compensation, which are two most sensitive resistors. The variation of \( R_1 \) and \( R_2 \) is 5% by using trimming as shown in Table IV.

<table>
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<tr>
<th>Resistor</th>
<th>Trimming Range</th>
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<tr>
<td>( R_1 )</td>
<td>163KΩ - 178KΩ</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>28.67KΩ - 31.31KΩ</td>
</tr>
</tbody>
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Table IV
RESISTOR TRIMMING RANGE

Figure 11. Resistor Global Variation

Figure 12. Resistor Mismatch

Figure 13. Resistor Trimming

The effect of error amplifier input offset as large as 10mV is also simulated as shown in Figure 14 and Figure 15. The relative variation is still within tolerance but the absolute value can exhibit significant change. As a consequence, resistor trimming has to be used for the output resistor or for the following circuit stages that uses this bandgap output.

CONCLUSION

A bandgap reference of \( V_{ref} \) 820mV with TC of 3ppm over \(-117^\circ C\) to \(144^\circ C\) is presented. The circuit uses tsmc 0.18\( \mu \)m technology and can virtually be fabricated using any standard CMOS technology as it uses only substrate PNP BJTs as reference generators. The process variations and mismatches
of resistors are compensated using trimming circuitry. Error Amplifier input offset effects are shown to affect the relative voltage variation only negligibly but induces DC offset at the output voltage. Trimming of the output resistor is required if the following stage needs an absolute voltage reference. The minimum supply voltage required is 1.3V and the circuit dissipates 28uA current. The chip area is estimated as 280 µm ×260 µm.

REFERENCES


